BS

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/768,589 | 01/25/2001 | Yoshizumi Haraguchi | PF-2723/NEC/US/mh | 3832 |

466 7590 06/17/2004

YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

| EXAMINER | |
|---|---|
| MISLEH, JUSTIN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2612 | 5 |

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/768,589 | HARAGUCHI, YOSHIZUMI | |
| | Examiner | Art Unit | |
| | Justin P Misleh | 2612 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) 1 - 7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 4 - 7 is/are allowed.

6)☒ Claim(s) 1 is/are rejected.

7)☒ Claim(s) 2 and 3 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 January 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. The Applicant is reminded of the proper language and format for an abstract of the disclosure. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. **The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided.** The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

More specifically, the abstract contains the words "comprises" and "wherein", which is considered by the Examiner as legal phraseology.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claim 1** is rejected under 35 U.S.C. 102(b) as being anticipated by Kawamoto et al.

5. For **Claim 1**, Kawamoto et al. disclose, as shown in figure 4 and as stated in column 7 (lines 43 – 67) and 8 (lines 1 – 29), a circuit (106) for processing charge detecting signal transferred to a floating diffusion amplifier (123) from a charge coupled device (101), said circuit (106) comprising:

a first node (the junction between the switching transistor Tr and the gate electrode 123 of the floating gate; see column 8, lines 18 – 29) connected to said floating diffusion amplifier (123);

a first enhancement type field effect transistor (Q1) being connected in series between a first fixed-voltage supply line (Vdd) for supplying a first fixed voltage and an output terminal (Φout), and said first enhancement type field effect transistor (Q1) having a first gate connected to said first node (see figure 4 and column 8, lines 1 – 10); and

a second enhancement type field effect transistor (Q2) being connected in series between a second fixed-voltage supply line (Vss) for supplying a second fixed voltage and the output terminal (Φout),

wherein said second enhancement type field effect transistor (Q2) has a second gate supplied with a third fixed voltage (Vgg) which is different in potential from said second fixed voltage (Vss).

Both the first and second enhancement type field effect transistors (Q1 and Q2) are in fact enhancement type transistors because both transistors require a gate voltage to open the channel between the drain and source of each of the transistors respectively.

Furthermore, Kawamoto et al. states in column 8 (lines 61 – 67), that the third fixed voltage (Vgg) is supplied to the gate of the second transistor (Q2) and that it is a bias voltage that may be changed to changed the gain of the G of the circuit (106) so that it may approach unity. If the third fixed voltage (Vgg) was equal to the second fixed voltage (Vss), it would be impossible to bias the second transistor (Q2) as described.

***Allowable Subject Matter***

6. **Claims 2 and 3** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. For **Claim 2**, the closest prior art teaches, at least of, a circuit comprised of a first enhancement type field effect transistor being connected in series between a first fixed-voltage supply line for supplying a first fixed voltage and an output terminal and a second enhancement type field effect transistor being connected in series between a second fixed-voltage supply line for supplying a second fixed voltage and the output terminal, wherein said second enhancement type field effect transistor has a second gate supplied with a third fixed voltage which is different in potential from said second fixed voltage. However, the closest prior art does not teach or fairly suggest wherein said second gate of said second enhancement type field effect transistor is connected to said first fixed-voltage supply line, and said second gate is supplied with said third fixed voltage which is equal to said first fixed-voltage.

8. **Claims 4 – 7** are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

For **Claim 4**, the closest prior art teaches, at least of, a circuit comprised of a first enhancement type field effect transistor being connected in series between a first fixed-voltage supply line for supplying a first fixed voltage and an output terminal and a second enhancement type field effect transistor being connected in series between a second fixed-voltage supply line for supplying a second fixed voltage and the output terminal, and said second enhancement type field effect transistor has a second gate connected to a second node. However, the closest prior art does not teach or fairly suggest a voltage control circuit being connected to said second node for connecting said second node to a third fixed-voltage in a first time period, in which said transfer clock signal is not supplied, and also for electrically isolating said second node from said third fixed-voltage in a second time period, in which said transfer clock signal is supplied.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following is a brief description of each of the cited prior art.

- **US 6,437,378 B1** discloses, as shown in figure 3, a second enhancement type field effect transistor (M3) that has a second gate connected to a second node (Vg).
- **US 6,465,819 B2** discloses, as shown in figure 11, a second enhancement type field effect transistor (L2) that has a second gate connected to the gate of a third enhancement type field effect transistor (L1).
- **US 6,243,434 B1** discloses, as shown in figure 7, a second enhancement type field effect transistor (Q3) that has a second gate connected to the second drain of the same field effect transistor.

- **US 5,033,068** discloses, as shown in figure 2, a second enhancement type field effect transistor (32) that has a second gate connected to ground (Vss) via a capacitor (33).
- **JP 05-136396** discloses, as shown in figure 1, a second enhancement type field effect transistor (22) that has a second gate connected directly ground.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 703.305.8090. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:30 PM and on alternating Fridays from 7:30 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 703.305.4929. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
June 7, 2004

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600